AzureWave Technologies, Inc.

AW-CU485

IEEE802.15.4 Wireless Microcontroller
Zigbee 3.0 Stamp LGA Module

Layout Guide

Rev. A

Revision History

Version	Revision Date	Description	Initials	Approved
A	2020/9/7	● Initial Version	Shihhua Huang	N.C. Chen

1. INTRODUCTION

This document provides key guidelines and recommendations to be followed when creating AW-CU485 layout. It is strongly recommended that layout be reviewed by AzureWave engineering team before released for fabrication.

The following is a summary of the major items that are covered in detail in this application note. Each of these areas of the layout should be carefully reviewed against the provided recommendations before the PCB goes to fabrication.

- Ground Layout
- Power Layout
- Digital Interface
- RF Trace
- The other layout guide Information
- Module stencil and Pad opening Suggestion

2. Ground Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

(1) The top layer of customer platform should keep **complete ground plane as possible as you can, in order to be connected for all ground pins of AW-CU485 module**.

(2) The area under our module forbidden any trace and via on top layer of customer platform.

3. Power Layout

Please follow general power layout guidelines. Here are some general rules for customers' reference.

(1) Power traces shall surround ground to get stable and make sure all power traces have good return path to ground.

(2) Do not get close to digital traces (SDIO.USB) or continuous data traces, there could be coupling noise affect power traces and IC.

4. Digital Interface

Please follow power and ground layout guidelines. Here are some general rules for customers' reference.

(1) The digital Interface to the module must be well routed to minimize coupling to power planes and other digital signals.

(2) SDIO and UART Traces need GND surrounded.

(3) SDIO pin can add pull high resistor on traces close WIFI module.(reserved solution)

(4) SDIO and UART traces between host and module are shot as possible.

(5) SDIO Traces length between host and module is equal as possible.

(6) SDIO & UART traces as possible away from CLOCK signal

5. RF Trace

The RF trace is the critical to route. Here are some general rules for customers' reference.

(1) The RF trace impedance should be 50Ω between ANT port and antenna matching network.

(2) The length of the RF trace should be minimized.

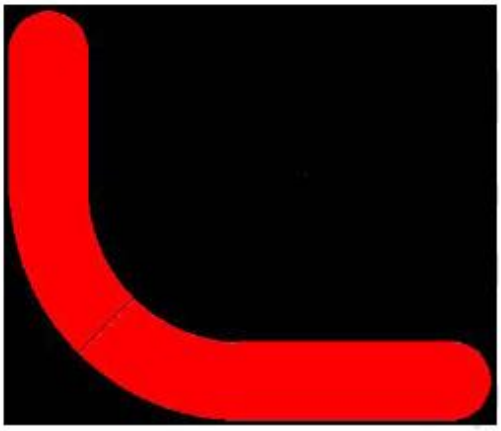
(3) To reduce the signal loss, RF trace should laid on the top of PCB and avoid any via on it.

(4) The CPW (coplanar waveguide) design and the microstrip line are both recommended; the customers can choose either one depending on the PCB stack of their products.

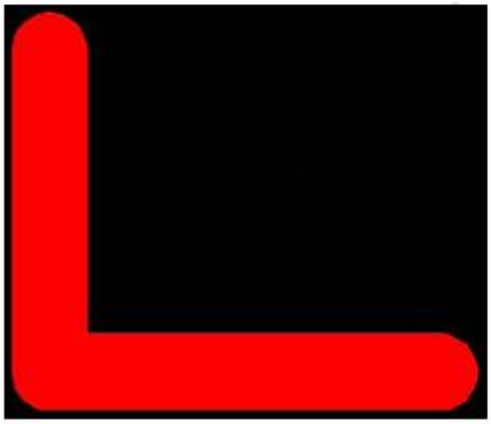
(5) The RF trace must be isolated with aground beneath it. Other signal traces should be isolated from the RF trace either by ground plane or ground vias to avoid coupling.

(6) To minimize the parasitic capacitance related to the corner of the RF trace, the right angle corner is not recommended.

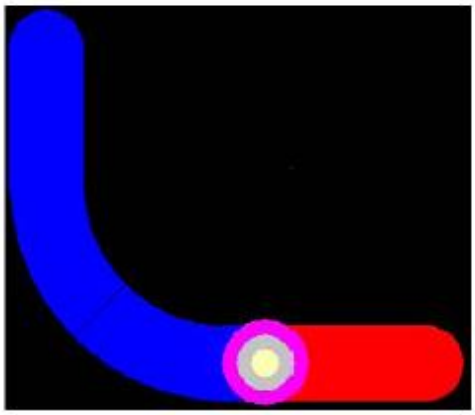
If the customers have any problem in calculation of trace impedance, please contact Azurewave.



Correct RF trace



Right-angled corner



Via on RF trace

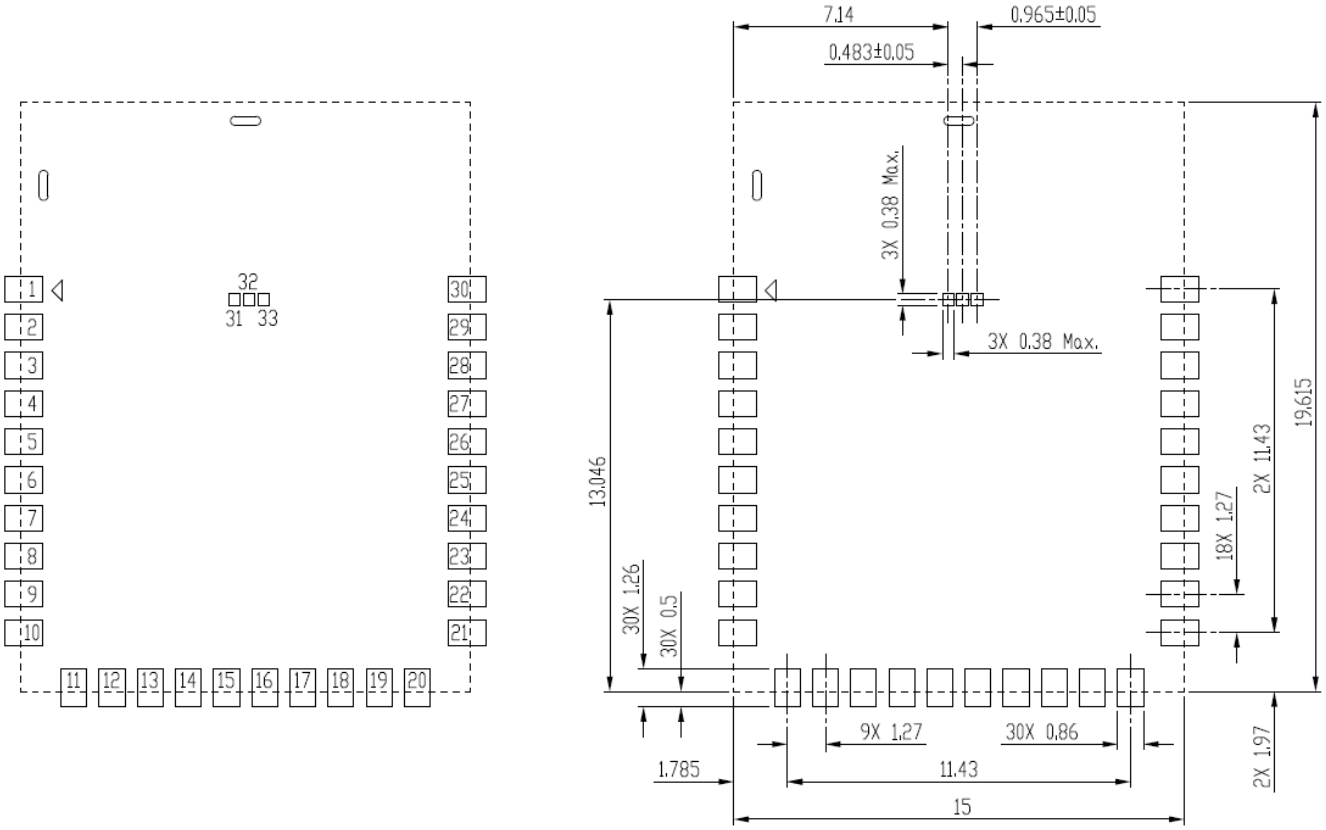
Incorrect RF trace

6. The other layout guide Information

- Keep the module unused function pins floating.
- High speed interface (i.e. UART/SDIO/HSIC) shall have equal electrical length. Keep them away from noise sensitive blocks.
- Good power integrity of VDD will improve the signal integrity of digital interfaces.
- Clock (SUSCLK) should have complete ground to make sure coupling will not happen to any other path.

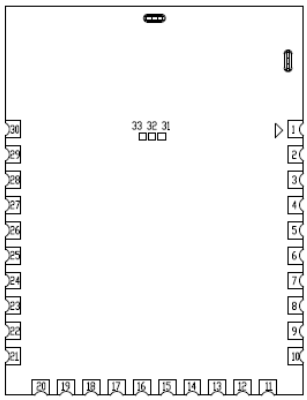
7. Module stencil and Pad opening Suggestion

- Function Pad opening size suggestion

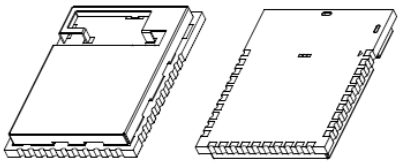


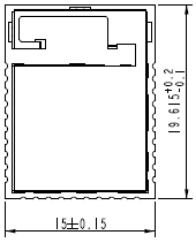
TOLERANCE UNLESS OTHERWISE SPECIFIED: ±0.1mm

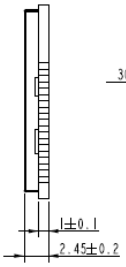
9. Mechanical Drawing

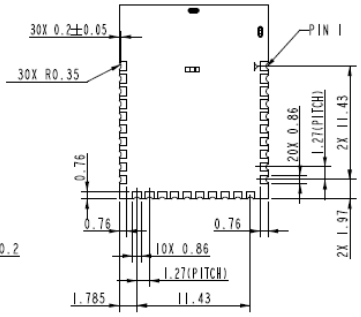


PIN DEFINED (BOTTOM VIEW)









TOLERANCES UNLESS OTHERWISE SPECIFIED:±0.1mm

			AzureWave					MODEL NO.		DESCRIPTION					DOCUMENT LEVEL	
								2480		OUTLINE DRAWING					NORMAL	
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ITEM	DESCRIPTION	DATE	TOL.	±0.1	±0.15	±0.20	±0.25		R2-2480-COD-01		mm	2/1	B	1/1	2020/04/29	STEVE CHANG